OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SUMMER EXAMINATIONS 2002

BSc Honours

Computer Science

CS4034 Embedded Systems Design

Professor J. G. Hughes
Professor C. J. Sreenan
Dr. Richard P. Studdert

Answer all questions
(Total 70 Marks)

Time 1 1/2 Hours

1 (a) The drive capability of the address output of a microprocessor IC is as follows: It can source 400μA at logic high and can sink 2mA at logic low. It is to be connected to ICs whose total load is I_{IH} = +2mA and I_{IL} = -18mA. A buffer IC is available whose DC characteristics (using the usual notation) according to the relevant data sheet are as follows:

I_{IH} = + 20μA, I_{IL} = - 400μA
I_{OL} = + 24mA, I_{OH} = - 2.6mA

Show, using a diagram, how you would connect the buffer IC between the microprocessor and the load. Clearly show on the diagram the source and sink currents at the various pins and state whether the buffer provides sufficient drive capability for the load. (5 Marks)

(b) The address lines of a particular microprocessor are multiplexed with the data lines. When the address issued by the processor is stable, the processor drives a control output from low to high. Show, with the aid of a suitable diagram, how you would demultiplex an address line from the corresponding data line. (5 Marks)

(c) Show, using a logic schematic, how you would provide buffering of a processor bidirectional data line. (5 Marks)

(d) Show, with the aid of an appropriate schematic, how you would interface an 8-bit input device using handshaking to the buffered bus of a processor that uses separate I/O addressing. (7 Marks)

2 (a) You are engaged to design a μ-processor based single board (SBC) computer system that will be used, not only as a stand alone target system, but also during the development stage when it will be connected to a PC. The board should have versatile parallel and serial I/O capability in addition to the μ-processor and EPROM and RW memory. Using generic style blocks to illustrate the individual functional hardware components, draw a system level diagram depicting the overall architecture of your system. Describe the software components that you would integrate onto the board and also on the PC to make your system suitable for use as a development system. (16 Marks)

(b) Discuss, with reference to the architecture of your I/O subsystem in (a) above or otherwise, the advantages of using interrupt versus polled I/O. (6 Marks)

3 (a) Show how data transparency is accomplished in bit oriented serial transmission. (5 Marks)

(b) The message frame, including the CRC field, received on a synchronous bit link is:

$$\text{msg + CRC} = 00101 \quad 11011 \quad 11110$$

The generator polynomial used is $G(x) = x^5 + x^4 + x^2 + 1$. Determine whether an error has occurred during transmission of the frame. (5 Marks)

(c) Explain, using frame sequence diagrams, how the Go-Back-N error control protocol caters for (i) a corrupted information frame and (ii) a corrupted acknowledge frame. Assume unlimited buffering at both ends of the link. (8 Marks)

(d) Briefly describe the sliding window protocol for flow control. Determine the send and receive window sizes when the sliding window flow control protocol is used in conjunction with the Go-Back-N error control protocol. Show that the use of flow control enables a finite number of distinct identifiers to be used and determine this minimum for both the Go-Back-N and Selective Retransmission control protocols. (8 Marks)

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AUTUMN EXAMINATIONS 2004

BSc Honours

Computer Science

CS4034 Embedded Systems Design

Professor Muffy Calder
Professor C. J. Sreenan
Dr. Richard P. Studdert

Answer all questions
(Total 70 Marks)

Time 1 1/2 Hours

1 (a) Show, using a logic schematic, how you would provide buffering of a processor bidirectional data line. *(8 Marks)*

(b) Show, with the aid of an appropriate schematic, how you would interface an 8-bit input device using handshaking to the buffered bus of a processor that uses separate I/O addressing. *(10 Marks)*

(c) Show, with the aid of an appropriate schematic, how you would expand your I/O system in (b) above to a number of I/P devices using polled I/O. *(12 Marks)*

2 (a) In the context of bit oriented synchronous serial transmission:
What levels of synchronisation are used, what is meant by data transparency and how is it accomplished? *(8 Marks)*

(b) The message frame, including the CRC field, received on a synchronous bit link is:

$$msg + CRC = 01001 \quad 11001 \quad 10111$$

The generator polynomial used is $G(x) = x^5 + x^4 + x^2 + 1$. Determine whether an error has occurred during transmission of the frame. *(5 Marks)*

(c) A satellite channel has a round trip propagation delay of 500 msec. If the Idle RQ protocol is used to send frames of 1000 bits at 50 kbps on the link, what is the link utilization? How could the link utilization be improved? *(7 Marks)*

3 Write a high level specification for the design of a time of day (real time) clock to be based on a 16 bit programmable counter. The initial value for time of day is to be input via a console keyboard. The current time of day is to be displayed on BCD (Binary Coded Decimal) seven segment displays attached to an 8255 PPI (Parallel Peripheral Interface) in the format hh:mm:ss.

The 4.9152Mhz clock input to the counter comes from the processor clock output. The counter output should be connected to a processor interrupt input, which interrupt should be used by a program to provide the one second timing resolution for the time of day clock.

Use flow diagrams to show the initialization and configuration of the I/O devices and the setup, operation and core elements, including the software, of the time of day clock. What determines the accuracy of the time of day display update? *(20 Marks)*